

N and P-Channel Enhancement Mode Power MOSFET



Description

The XPX06NP10XS uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge . The complementary MOSFETs may be used to form a level shifted high side switch, and for a host of other applications.

General Features

- High power and current handing capability
- Lead free product is acquired
- Surface mount package

V DS =100V,ID =6A RDS(ON)=130mΩ (typ) @ VGS=10V RDS(ON)=150mΩ (typ) @ VGS=4.5V V DS =-100V,ID =-6A RDS(ON)=135mΩ (typ) @ VGS=10V RDS(ON)=165mΩ (typ) @ VGS=4.5V



N-Channel MOSFET

P-Channel MOSFET

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
XPX06NP10XS	XPX06NP10XS	SOP-8	Ø330mm	12mm	3000

Absolute Maximum Ratings (T_A= 25°C unless otherwise noted)

Symbol	Parameter	N Chan	P Chan	Unit	
Common F	Ratings				
V_{DSS}	Drain-Source Voltage	100	-100	V	
V_{GSS}	Gate-Source Voltage	±20	±20	v	
T _j	Maximum Junction Temperature	1:	50	*0	
T _{STG}	Storage Temperature Range	-55 to 150		°C	
I _D	Continuous Drain Current		-6	А	
I _{DM}	Pulsed Drain Current	12	-12	А	
P _D	Power Dissipation 1.4				
$R_{ ext{ heta}JA}$	Thermal Resistance-Junction to Ambient		9.3	°C/W	
$R_{ ext{ heta}JC}$	Thermal Resistance-Junction to Case		3.8	°C/W	

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.



N-Channl Electrical Characteristics (T_A= 25°C unless otherwise noted)

Currente e l	Parameter	Test Conditions	N-Channl			Unit	
Symbol			Min.	Тур.	Max.	Unit	
Static C	haracteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =250μA	100	-	-	V	
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =80V, V _{GS} =0V	-	-	1	μA	
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_{DS} = 250 \mu A$	1		3	V	
I _{GSS}	Gate Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	±100	nA	
D		V _{GS} =10V, I _{DS} =3A	-	130	150	mΩ	
R _{DS(ON)}	Drain-Source On-state Resistance	V _{GS} =4.5V, I _{DS} =3A	-	150	185		
V _{SD}	Diode Forward Voltage	I _{SD} =6A, V _{GS} =0V	-	-	1.3	V	
Dynamic	Characteristics	•					
C _{iss}	Input Capacitance		-	923	-	pF	
C _{oss}	Output Capacitance	V _{GS} =0V, V _{DS} =25V, Frequency=1.0MHz	-	54	-		
C _{rss}	Reverse transfer capacitance		-	43	-		
t _{d(ON)}	Turn-on delay Time		-	3.5	-		
t _r	Turn-on rise Time	V _{GEN} =10V ,V _{DD} =50V R _G =25Ω, I _{DS} =6A	-	17	-	nS	
t _{d(OFF)}	Turn-off delay Time		-	22	-		
t _f	Turn-off rise Time		-	17	-		
Gate Ch	Gate Charge Characteristics						
Qg	Total Gate Charge		-	23	-		
Q _{gs}	Gate-Source Charge	V _{DS} =50V, V _{GS} =10V, I _{DS} =6A	-	3.4	-	nC	
Q_{gd}	Gate-Drain Charge		-	4.7	-		

Notes: 1. Pulse Test: Pulse width limited by Max. junction temperature. 2. N-CH, P-CH are same, mounted on 2oz FR4 board t \leq 10s.



P-Channi Electrical Characteristics ($T_A = 25^{\circ}C$ unless otherwise noted)

Cumhal	Parameter	Test Conditions	1	P-Channl			
Symbol			Min.	Тур.	Max.	Unit	
Static C	Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =-250A	-100	-	-	V	
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-80V, V _{GS} =0V	-1	-	-1	μA	
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{DS} = -250A$	-1		-3	V	
I _{GSS}	Gate Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	±100	nA	
Р	Drain-Source On-state Resistance	V _{GS} =-10V, I _{DS} =-3A	-	135	155	mΩ	
R _{DS(ON)}		V _{GS} =-4.5V, I _{DS} =-3A	-	165	210		
$V_{\text{SD}}^{}\text{d}}$	Diode Forward Voltage	I _{SD} =-6A, V _{GS} =0V	-	-	-1.3	V	
Dynamic	Characteristics	·					
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-25V, Frequency=1.0MHz	-	1350	-	pF	
C _{oss}	Output Capacitance		-	90	-		
C _{rss}	Reverse transfer capacitance		-	62	-		
t _{d(ON)}	Turn-on delay Time		-	6.5	-		
t _r	Turn-on rise Time	V _{GEN} =-10V ,V _{DD} =-50V R _G =3.3Ω, I _{DS} =-6A	-	17	-	nS	
t _{d(OFF)}	Turn-off delay Time		-	37	-		
t _f	Turn-off rise Time		-	19	-		
Gate Ch	Gate Charge Characteristics						
Q _g	Total Gate Charge		-	34	-		
Q _{gs}	Gate-Source Charge	V _{DS} =-50V, V _{GS} =-10V, I _{DS} =-6A	-	5.2	-	nC	
Q_{gd}	Gate-Drain Charge		-	5.5	-	1	

Notes: 1. Pulse Test: Pulse width limited by Max. junction temperature. 2. N-CH, P-CH are same, mounted on 2oz FR4 board t \leq 10s.



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TYPICAL CHARACTERISTICS







N and P-Channel Enhancement Mode Power MOSFET

TYPICAL CHARACTERISTICS (Cont.)











Source-Drain Voltage, V_{SD} (V)





TYPICAL CHARACTERISTICS (Cont.)

P-CHANNEL





TYPICAL CHARACTERISTICS (Cont.)















N and P-Channel Enhancement Mode Power MOSFET

TYPICAL CHARACTERISTICS (Cont.)





Vos

VDD

VDD

N and P-Channel Enhancement Mode Power MOSFET

Avalanche Test Circuit and Waveforms



Switching Time Test Circuit and Waveforms

N Channel





90% Vds





N and P-Channel Enhancement Mode Power MOSFET

SOP8 PACKAGEE OUTLINE









字符	Dim	ension millimete	ers
7-17	Min	Standard	Max
Α	1.39	1.55	1.700
A1	0.04	0.08	0.15
A2	1.350	1.450	1.550
b	0.300	0.400	0.500
с	0.220	0.254	0.280
D	4.800	4.900	5.000
Е	3.840	3.940	4.040
E1	5.900	6.000	6. 100
е		1.27 (BSC)	
L	0.400	0.550	0.700
θ	0°		8°



Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃ ±5 ℃	5sec±1sec
Pb-Free device	260 ℃ +0/-5 ℃	5sec±1sec



This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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